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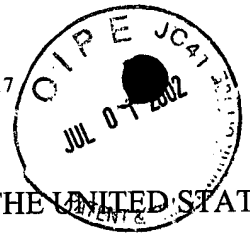

Attorney Reference Number 6047-61248
Application Number 09/971,952

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Prindiville et al.

Art Unit: 2827

Application No. 09/971,952

Filed: October 4, 2001

For: SEMICONDUCTOR PACKAGES AND METHODS FOR MAKING THE SAME

Examiner: Lourdes C. Cruz

Date: June 24, 2002

CERTIFICATE OF MAILING

I hereby certify that this paper and the documents referred to as being attached or enclosed herewith are being deposited with the United States Postal Service on June 24, 2002 as First Class Mail in an envelope addressed to: COMMISSIONER FOR PATENTS, WASHINGTON, D.C. 20231.

Wayne W. Rupert
Attorney for Applicant

COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

REPLY TO OFFICE ACTION

This is a reply to a non-final Office Action mailed March 22, 2002. A reply is due by June 22, 2002, which is a Saturday, making the reply due by June 24, 2002. Reconsideration and withdrawal of the pending rejections is respectfully requested. A Letter to the Official Draftsperson submitting corrected drawings of FIGS. 1A, 3A and 3B accompanies this reply.

In the claims:

Please add the following claims:

B'

36. (New) The defective semiconductor package of claim 30, wherein the cover member covers from about 70% to about 98% of the opening formed by the wire bond slot.

37. (New) The defective semiconductor package of claim 30, wherein the wire bond slot is associated with the defective die attach site.

38. (New) The defective semiconductor package of claim 30, wherein the cover member comprises a defective die.

39. (New) The defective semiconductor package of claim 30, wherein the cover member covers from about 80% to about 90% of the opening formed by the wire bond slot.

40. (New) The defective semiconductor package of claim 30, wherein the cover member covers at least about 70% of the opening formed by the wire bond slot.

REMARKS

The Official Action mailed March 22, 2002, has been reviewed and the comments of the PTO carefully considered. Claims 36-40 have been added. Support for claims 36, 39 and 40 is found in the specification at page 8, lines 15-20. Support for claim 37, is found in the specification at page 6, lines 25-29. Support for claim 38 is found in the specification at page 7, lines 19-20. Entry of these new claims is respectfully requested.

Claims 30-32 have been rejected under §102(e) over Eng et al. The Examiner asserts that element 60 of the Eng et al. package is a cover member as recited in claim 30. However, upon closer inspection it is clear that element 60 is not a cover member that covers "at least a portion of the opening" as recited in claim 30. Element 60, in fact, is an adhesive layer that adheres the printed circuit board 70 to the silicon chip 50 (see column 3, lines 33-35). The adhesive layer may be a two-sided adhesive tape, but there is no indication in Eng. et al. that the adhesive layer 60 should cover at least a portion of opening 86 formed in the substrate 76. Indeed, FIG. 1 of Eng et al. shows the adhesive layer 60 as being co-extensive with the opening 86. Accordingly, the §102(e) rejection of claim 30-32 over Eng et al. should be reconsidered and withdrawn since Eng et al. does not disclose all the presently claimed features. Applicants also note that in another divisional application (Serial No. 09/971,872) corresponding to the present application, the PTO has appreciated that Eng et al. fails to disclose "a cover member attached to the substrate on the second surface so as to cover at least a portion of the wire bond slot, wherein the cover member does not comprise a functional die" (see Office Action mailed January 30, 2002, page 3).

Claims 30-32 also have been rejected under §103 over Eng et al. combined with Vindasius et al. Vindasius et al. is relied upon for allegedly disclosing defective die attach sites. Column 4, lines

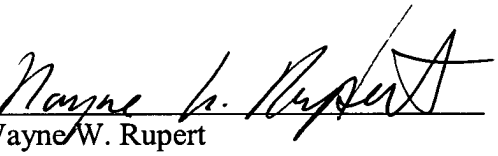
17-19, of Vindasius et al. state that "Wafers 30 normally arrive from the manufacturer with non-functioning or defective die which are marked with an ink dot 34." Thus, Vindasius et al. discloses defective dies rather than defective die attach sites. In claim 30, the aspect that is defective is the die attach site, not the die itself. This construction is consistent with the specification which states, for example, that "The die attach area of each substrate 56 comprises either an 'operational' or 'functional die site' 50 or a 'defective' of 'reject die site' 36" (see page 6, lines 11-16). Vindasius et al. is not concerned with defective die attach sites, and therefore the §103 rejection over Eng et al. combined with Vindasius et al. should be reconsidered and withdrawn.

The pending §103 rejection should be reconsidered and withdrawn for the foregoing reason alone, but applicants also note that Vindasius et al. does not cure the above-discussed fatal deficiency in Eng et. al. regarding the lack of a cover member. Moreover, there would have been no motivation to extend the adhesive layer 60 of Eng et al. to cover at least a portion of the opening 86. Adhesive layer 60 adheres the printed circuit board 70 (via substrate 76) to the silicon chip 50. There would have been no reason to extend the adhesive layer 60 to an area where substrate 76 does not exist (i.e., opening 86) because a non-functional extended adhesive area would be unnecessary.

Accordingly, it is respectfully submitted that the present claims are in condition for allowance. Should there be any questions regarding this application, Examiner Cruz is invited to contact the undersigned attorney at the telephone number shown below.

Respectfully submitted,

KLARQUIST SPARKMAN, LLP

By 
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